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| Grade | TG. | Breadth | Depth | Presentation | Understanding |
| A/A\* |  | ALL | **LINK / FORMULATE**  Create, Generate, Hypothesis, Reflect, Theorise, Consider | Quad  Core | Quad  Core |
| B/C |  | MOST | **EXPLAIN / ANALYSE**  Apply, Argue, Compare, Contrast, Criticise, Relate, Justify | Dual  Core | Dual  Core |
| D/E |  | SOME | **DESCRIBE / IDENTIFY**  Name, Follow Simple Procedure, Combine, List, Outline | Single  Core | Single  Core |
| U |  | FEW | Very little depth of understanding shown |  |  |
|  |  | **MY ASSESSMENT GRADE IN THIS TOPIC IS:** | | | |



**1 - Structure and function of the processor (AS / A Level)**

**UNIT 1**

**Examination Questions**

1. Describe the stages of the fetch-decode-execute cycle.

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1. Increasing the number of cores affects the performance of the CPU. Explain why this increase in performance is not linear.

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1. State the purpose of the address bus.

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1. Name one register other than the PC found in the CPU and describe its purpose.

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1. Explain why the Little Man Computing (LMC) instructions BRA / BRP would cause the contents of the PC to change.

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How To Improve:

**My Response Is:** (Set yourself specific targets / objectives as to how you will achieve your HTI)

Expectations / Learning Outcomes:

* Terms 1-21 from your **A Level Key Terminology** PowerPoint should be included and underlined.
* You must include at least one diagram which depicts the fetch-decode-execute cycle.
* You must include at least one diagram which shows the direction and connections of the 3 busses.
* You must include at least one diagram which illustrates how the various registers interact during a typical fetch-decode-execute cycle.

Specification Points / Learning Objectives: **Core text book page ref: 124-131, 133-134**

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| **AS Level** | **A Level** | **Specification point description** |
| 1.1.1a | 1.1.1a | The arithmetic logic unit; ALU, Control Unit and Registers (Program Counter; PC, Accumulator; ACC, Memory Address Register; MAR, Memory Data Register; MDR, Current Instruction Register; CIR). Busses: data, address and control: How this relates to assembly language program |
| 1.1.1b | 1.1.1b | The fetch-decode-execute cycle, including its effect on registers |
| 1.1.1c | 1.1.1c | The factors affecting the performance of CPU, clock speed, number of cores, cache |
|  | 1.1.1d | The use of pipelining in a processors to improve efficiency |
| 1.1.1d | 1.1.1e | Von Neumann, Harvard and contemporary processor architecture |